Claims

1. Circuit arrangement for controlling a brushless, permanently excited direct current motor (BLDC motor, 1), having a rotor, a stator and a plurality of Phases(P1, P2, to Pn) with in each case an external phase connection (V1, V2, to Vn),

- having a power control unit (6), to which the phases and a power DC voltage source (5) are connected and by which the phases are electrically connected to a higher or lower voltage potential of the power DC voltage source (5) or are electrically separated from both potentials,

- having a main control unit (4) which is electrically connected to the phase connections and to the power control unit (6), and whereby said main control unit (4) controls the power control unit (6), as a function of an electrical induction signal (U1) induced in a signal phase (P1) of the motor by the rotation of the rotor, in such a way that the phases dependent on the relative rotational position of the rotor are electrically connected in cyclic sequence (P1, P2, P3, to Pn or Pn, to P3, P2, P1), and offset in time, for a commutation interval in each case, alternating between a higher or lower voltage potential of the power DC voltage source (5) or are electrically separated from both potentials,

characterized by

- a capacitive interference suppression component (CR), arranged immediately between the external phase connection(V1) of the signal phase (P1) on which the induction signal (U1) is present and the external phase connection (V2 or Vn) of one of the adjacent phases (P2 or

Pn) in the electrical cycle, the interference suppression component (CR) acting as part of a bridge circuit in which the signal phase (P1) forms the measuring bridge, and the bridge circuit having the following components:

a) both the phases (P2 and Pn) adjacent to the signal phase (P1),

b) a spurious total capacitance ($2xC_P$) of the electronic components (C_P) of the power control which are assigned to the signal phase,

c) the signal phase (P1) and

d) the interference suppression component (CR).

2. Circuit arrangement according to claim 1, characterized by a pulse width generator which provides pulse-width modulated control signals that are used to make the electrical connection between the phases and the higher or lower potential of the power DC voltage source during the commutation interval with pulse-width modulation in a variable pulse-width ratio.

3. Circuit arrangement according to claim 1 or 2, characterized by a half-wave differential amplifier unit with filter function, connected input-side to the phase connections (V1, V2 and Vn) of the signal phase (P1) and both adjacent phase (P2 and Pn) in the electrical cycle, and having an output-side signal line (DA1), on which an evaluation signal (us) is present, which is proportional to the induction signal (U1) of the signal phase (P1).

4. Circuit arrangement according to one of the claims 1 to 3, characterized by a gate generator which is connected to the signal phase (P1) or to a signal line (VS) on which the induction signal (U1) or the evaluation signal (us) is present, and

- which serves to mask the induction signal (U1) or the evaluation signal (us) in accordance with an open-window control signal (owd), defining a period of observation in the electrical cycle in which the evaluation signal (us) can be measured.

5. Circuit arrangement according to claim 4, characterized by a signal generator for the open-window control signal (owd),
- which is connected input-side to the signal line on which the evaluation signal is present, and to the main control unit(4), and
- by means of which the open-window control signal (owd), in accordance with a no-load signal (nss) which is proportional to the evaluation signal (us) present on the signal line, and also by means of a state-window signal (swd) generated by the control unit, is set, the minimum duration of the period of observation being predefined by the state-window signal (swd) from the control unit.

6. Circuit arrangement according to one of the claims 1 to 5, characterized by a position detector for generating a position signal (up)
- which is connected input-side to the signal phase (P1) or the signal line (VS) on which the induction signal (U1) or the evaluation signal (us) is present, and to at least one further signal line on which a threshold signal (ut) is present,
- the position signal (up) that is present on the signal output (PA1) of the position detector being dependent on the comparison of the induction signal (U1) or the evaluation signal (us) with the predetermined threshold signal (ut).

7. Circuit arrangement according to claims 4 and 6, characterized by a threshold generator
- which is connected input-side to the main control unit (4)

and output-side to the position detector,
- said threshold generator only raising the threshold signal (ut) at the start of the period of observation, depending on request signals (sax) from the control unit and an activation signal (uta).

8. Method for controlling a brushless, permanently excited direct current motor having a circuit arrangement for controlling according to claim 1,
- the phases dependent on the relative rotational position of the rotor being electrically connected in cyclic sequence (P1, P2, P3, to Pn or Pn, to P3, P2, P1), and offset in time, for a commutation interval in each case, alternating between a higher or lower voltage potential of a power DC voltage source (5), or being electrically separated from both potentials,
- the relative rotational position of the rotor being determined with the aid of the induction signal (U1) present on the signal phase (P1), characterized in that the electrically capacitive interference suppression component(CR) is so dimensioned that a bridge circuit is balanced, and has the following components:

a) both the phases (P2 and Pn) adjacent to the signal phase,
b) a spurious total capacitance ($2xC_P$) of the electronic switches which are assigned to the signal phase (P1),
c) the signal phase (P1) itself and
d) the electrically capacitive interference suppression component (CR) and

in which the signal phase (P1) forms the measuring bridge, for which reason the interfering influences on the induction signal (U1) caused by the electronic switches (C_p) of the signal phase (P1), are compensated for by the interference suppression component.

9. Method according to claim 8, characterized in that the electrical connection between the phases (P1, P2, P3,...Pn) and the higher or lower potential of the power DC voltage source (5) is made during the commutation interval with pulse-width modulation in a variable pulse-width ratio.

10. Method according to claim 8 or 9, characterized in that the induction signals (U1, U2 and Un) of the signal phase (P1) and the two adjacent phases (P2 and Pn) in the electrical cycle are linked together by circuitry or by a computer program in the control unit in such a way that high-frequency interfering influences superimposed on the induction signal are filtered out, resulting in an evaluation signal (us) expressed by the relationship

$$us = \left(\frac{n-1}{n}\right) \cdot U1 - \frac{1}{n} \cdot \sum_{\omega=1}^{n} U_{\omega}$$

said signal being referenced to the 0V potential of a circuit DC voltage source (3), used to supply electrical power to the circuit arrangement, where n represents the number of phases and U_{ω} the induction signal on the phase concerned.

11. Method according to one of the claims 8 to 10, characterized in that the induction signal (U1) of the signal phase (P1) or the evaluation signal (us), in accordance with an open-window control signal (owd) is overlaid with a potential of the circuit DC voltage source (3), for which reason a period of observation is defined in relation to time, in the region of which the induction signal (U1) the signal phase (P1) or the evaluation signal (us) can be measured.

12. Method according to claim 11, characterized in that the open-window control signal (owd), in accordance with a no-load

signal (nss) which is proportional to the induction signal (U1) of the signal phase (P1) or to the evaluation signal (us), and also by means of a state-window signal (swd) generated by the control unit, is set, the minimum duration for which the open-window control signal (owd) remains set being predefined by the state-window signal (swd) from the control unit.

13. Method according to one of the claims 8 to 12, characterized in that the position signal (up) results from comparison of the induction signal (U1) of the signal phase (P1) or the evaluation signal (us) with a predefined threshold (ut) within the period of observation, a switching signal (uss) being generated only when the value drops below the threshold (ut) for a predefined interval, the value of said switching signal exceeding the response threshold of a switching element (ST), for which reason the position signal (up) is generated at its output.

14. Method according to claim 13, characterized in that the desired value of the threshold (ut) is adjustable within a range, dependent on control signals (sax) of the control unit, and the induction signal (U1) or the evaluation signal (us) falls below the threshold (ut) within the period of observation in the electrical cycle sooner in the case of a higher threshold and later in the case of a lower threshold.

15. Method according to one of the claims 13 or 14, characterized in that the threshold (ut) is raised with delay to its desired value only at the start of the period of observation, depending on an activation signal (uta), thus preventing a premature fall below the threshold.

16. Method according to claim 15, characterized in that the open-window control signal (owd) is used as an activation signal (uta).

17. Method according to one of the claims 8 to 16, characterized in that to produce the method according to one of the claims 8 to 16 the control unit is used in such a way that at least one of the features of the method is put into effect by computer algorithms programmed in the control unit.